**POORNIMA UNIVERSITY, JAIPUR.**

**END SEMESTER EXAMINATION, April 2023**

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|  | **1BC2156** | Roll No. | Total Printed Pages: 2 |
| **1BC2156** |  |
| BCA I Year II Semester (Back) End Semester Examination, April 2023  **(All Spl.)** | |
| **BADCCA2102 /BCSCCA2102 /BCMCCA2102 / BCTCCA2102: Computer Organization & Architecture** | | | |

# Max. Time: **3** Hours. Max. Marks: **60**

Min. Passing Marks: **21**

Attempt **five** questions selecting one question from each Unit. There is internal choice from Unit I to Unit V. Marks of each question or its parts are indicated against each question / parts. Draw neat sketches wherever necessary to illustrate the answer. Assume missing data suitably (if any) and clearly indicate the same in the answer.

Use of following supporting material is permitted during examination for this subject.

# **1.----------------------------------------------** **2.-----------------------------------------**

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|  |  | **UNIT-I (CO1)** | **Marks** | **Bloom Level** |
| **Q.1** | **(a)** | Discuss the register transfer and RTL and illustrate to  represent the following conditional control statement(s) by two register transfer statements with control function.  If (P=1) then (R1 ← R2) else if (Q=1) then (R1 ← R3) | **(6)** | **Analyze** |
|  |  |  |  |  |
|  | **(b)** | Assume the values of A and B and Justify the binary number system, B - A is equivalent to B + A' + 1. | **(6)** | **Evaluate** |
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|  |  | **OR** |  |  |
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| **Q.2** | **(a)** | Elaborate the block diagram of 4-bit adder-subtractor circuit. Discuss with the help of a suitable example. | **(6)** | **Apply** |
|  |  |  |  |  |
|  | **(b)** | Construct a common bus system using multiplexers for 4 Registers. | **(6)** | **Apply** |
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|  |  | **UNIT-II (CO2)** |  |  |
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| **Q.3** | **(a)** | Give an example of register transfer of data through accumulator. Justify the example with the instruction format type and assembly language code. | **(6)** | **Analyze** |
|  |  |  |  |  |
|  | **(b)** | Consider R1=1101 and R2=0111 Design and explain Binary Incrementor circuit for R1 | **(6)** | **Apply** |
|  |  |  |  |  |
|  |  | **OR** |  |  |
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| **Q.4** | **(a)** | Draw a flowchart to justify the distinct phases of Instruction Cycle in detail | **(6)** | **Understand** |
|  |  |  |  |  |
|  | **(b)** | Justify the concept of direct and indirect addressing modes to show how the different types of operands that can appear in an instruction with the help of a block diagram. | **(6)** | **Knowledge** |
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|  |  | **UNIT-III (CO3)** |  |  |
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| **Q.5** | **(a)** | Establish how control signals are generated using micro-programmed and hardwired control. | **(6)** | **Analyze** |
|  |  |  |  |  |
|  | **(b)** | Briefly examine the notion of Control Word. Draw the architecture for Control Word Sequencing. | **(6)** | **Understand & apply** |
|  |  | **OR** |  |  |
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| **Q.6** | **(a)** | Examine the roles of various components employed in the construction of Control Unit (CU). Build the organizational flow of each of the components in the designing of CU. | **(6)** | **Understand** |
|  |  |  |  |  |
|  | **(b)** | Elaborate the Hardwired Control Unit with the help of a block diagram | **(6)** | **Understand** |
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|  |  | **UNIT-IV (CO4)** |  |  |
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| **Q.7** | **(a)** | Assume 5-bit registers that hold signed numbers. Compute the expression: (+10) X (-13) using Booth’s Algorithm. | **(6)** | **Evaluate** |
|  |  |  |  |  |
|  | **(b)** | Discuss microoperations and show Decrement operation using 2’s complement with the help of a suitable example. Perform the arithmetic operation in binary using 2’s complement representation: (i) (+62) + (-3) (ii) (-12) – (-13). | **(6)** | **Evaluate** |
|  |  |  |  |  |
|  |  | **OR** |  |  |
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| **Q.8** | **(a)** | Derive an algorithm in flow chart form for the Restoring method of fixed-point binary division | **(6)** | **Evaluate** |
|  |  |  |  |  |
|  | **(b)** | Consider the step-by-step process of Booth’s algorithm for solving (-7) X (+3). Assume the register Size to be 5. | **(6)** | **Evaluate** |
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|  |  | **UNIT V (CO5)** |  |  |
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| **Q.9** | **(a)** | Emphasize the usage of DMA controller in a computer system with a neat diagram. | **(6)** | **Understand** |
|  |  |  |  |  |
|  | **(b)** | In what way the main memory is useful in computer system? Illustrate the memory address map of RAM and ROM | **(6)** | **Analyze** |
|  |  |  |  |  |
|  |  | **OR** |  |  |
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| **Q.10** | **(a)** | Discuss the different modes of Data Transfer. Write the pros and cons of using programmed I/O mode. | **(6)** | **Analyze** |
|  |  |  |  |  |
|  | **(b)** | Write short note on Cache memory and discuss the associative mapping in organization of cache memory | **(6)** | **Understand** |